Remarks/Arguments

Applicants have received the Final Office Action dated February 27, 2007, in which the Examiner: 1) rejected claims 1-8 under 35 U.S.C. §112, 1st paragraph, as allegedly failing to comply with the written description requirement, 2) rejected claims 1-8, 12-13 and 19 under 35 U.S.C. §103(a) as allegedly obvious under Adams (U.S. Pat. No. 6,151,661) in view of Lopriore ("Line Fetch/Prefetch in a Stack Cache Memory") and Handy ("The Cache Memory Book"), and 3) rejected claims 9-11, 14, 16-18 and 20 under 35 U.S.C. §103(a) as allegedly obvious under Adams in view of Lopriore. With this Amendment, Applicants amend claim 1. Based on the amendment and arguments herein, Applicants respectfully submit that all pending claims are in condition for allowance.

I. REJECTIONS UNDER 35 U.S.C. §112, 1st PARAGRAPH

The Examiner rejected claims 1-8 under 35 U.S.C. §112, 1st paragraph, as allegedly failing to comply with the written description requirement. In particular, the Examiner asserted that the limitation "determining whether the data is being removed from a dirty cache line in a cache memory" finds no support in the specification. Applicants have amended claim 1 to remove this limitation, not because Applicants agree with the Examiner's rejection, but because claim 1 is patentable even without this limitation, as explained below. Because this limitation has been removed from claim 1, Applicants kindly request the Examiner to remove this rejection.

II. REJECTIONS UNDER 35 U.S.C. §103(a)

A. Claims 1-8, 12-13 and 19

The Examiner rejected claims 1-8, 12-13 and 19 under 35 U.S.C. §103(a) as allegedly obvious under Adams in view of Lopriore and Handy. Amended claim 1 requires "if the data being removed corresponds to a predetermined word in a dirty cache line in a cache memory, queuing the dirty cache line for replacement..." (emphasis added). The combination of Adams, Lopriore and Handy fails to teach or suggest this limitation. In paragraphs 15 and 16 of the Final Office Action, the Examiner admits that Adams fails to disclose the above limitation in the context of dirty cache

lines (see, in particular, the last sentence of paragraph 16). The Examiner also fails to point out where Lopriore and Handy teach or even suggest the above limitations in the context of dirty cache lines. It appears that Lopriore and Handy fail to teach or even suggest this limitation in the context of dirty cache lines. Claim 1 and dependent claims 2-8 are patentable over the combination of Adams, Lopriore and Handy for at least this reason.

Claim 1 is patentable for an additional reason. In particular, claim 1 requires "...and not writing the dirty cache line to a memory external to a processor." The combination of Adams, Lopriore and Handy fails to teach or suggest this limitation. In paragraphs 17-19 of the Final Office Action, the Examiner asserts that it would have been obvious to not write a dirty cache line to main memory when the highest address word in the cache line is POPPED, as the cache line does not contain any valid data, and cites Adams and Lopriore for support. However, Applicants remind the Examiner that the cited teachings of the references are not directed to dirty cache lines, as is claim 1. Dirty cache lines generally are designated as "dirty" because they contain data which needs to be written to memory before the dirty cache line is invalidated or otherwise cleared for other data. Claim 1 distinguishes over prior art at least because it requires that the dirty cache line data not be written to memory before the dirty cache line is queued for replacement. In the apparent absence of a dirty cache line context in the cited references, the Examiner cannot presume sua sponte that the references' teachings would hold true for dirty cache lines. For at least this reason, claim 1 and dependent claims 2-8 are patentable over the combination of Adams, Lopriore and Handy.

Independent claim 9 requires "if data being removed comprises a predetermined word in a dirty cache line, the controller queues the dirty cache line to be overwritten, and wherein the dirty cache line is not saved to the main memory." As explained above in the context of claim 1, the combination of the cited references fails to teach or

suggest this limitation. For at least this reason, claim 9 and dependent claims 10-14 and 16 are patentable over the combination of Adams, Lopriore and Handy.

Independent claim 17 requires "if the processor reads a value from the top of the stack that comprises a word at a predetermined location within a dirty cache line in said cache memory, the cache controller queues said dirty cache line for replacement, and the dirty cache line is not written to a memory external to the processor." As explained above in the context of claim 1, the combination of the cited references fails to teach or suggest this limitation. For at least this reason, claim 17 and dependent claims 18-20 are patentable over the combination of Adams, Lopriore and Handy.

B. Claims 9-11, 14, 16-18 and 20

The Examiner rejected claims 9-11, 14, 16-18 and 20 under 35 U.S.C. §103(a) as allegedly obvious under Adams and Lopriore. However, as explained above, each of these claims is patentable over the art of record. Thus, this rejection is moot.

III. CONCLUSION

Applicants respectfully request reconsideration and that a timely Notice of Allowance be issued in this case. In the event that additional fees related to this Amendment, or other transactions in this case, are required (including fees for net addition of claims), the Examiner is authorized to charge Texas Instruments Inc.'s Deposit Account No. 20-0668 for such fees.

Respectfully submitted,

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